Please add new claims 30-33 as follows:

--30. (new) A semiconductor device comprising:

a semiconductor substrate including first and second memory cell areas;

the first memory cell area including a first horizontal field effect transistor comprising a first tunnel insulating film in contact with the substrate, a first floating gate in contact with the tunnel insulating film, a first dielectric layer in contact with the floating gate, a first control gate in contact with the dielectric layer, and first source/drain regions extending into the substrate;

the second memory cell area including a second horizontal field effect transistor comprising a second tunnel insulating film in contact with the substrate, a second floating gate in contact with the second tunnel insulating film, a second dielectric layer in contact with the second floating gate, a second control gate in contact with the second dielectric layer, and second source/drain regions extending into the substrate;

the first source/drain regions and the second source/drain regions each including an upper surface that extends along a common plane; and

a connecting area capable of electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the connecting area has an electric resistance which is lower than any of the source/drain regions.

31. (new) The semiconductor device according to claim 30, wherein a groove is formed on the connecting area on the semiconductor substrate.

32. (new) The semiconductor device according to claim 31, wherein no portion of the floating gate, no portion of the dielectric layer, and no portion of the control gate are positioned within the groove.